CHIP-SIZE SEMICONDUCTOR PACKAGE

【0001】

TECHNICAL FIELD OF THE INVENTION

The present invention generally relates to a chip-size semiconductor package, and more particularly to a chip-size semiconductor package having a wiring layer in which stress applied thereto is effectively relaxed.

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BACKGROUND OF THE INVENTION

Usually, a chip-size semiconductor package includes a Si chip; metal pads formed on the Si chip; a wafer coating formed over the Si chip; conductive wiring patterns formed on the wafer coating; a molding resin formed over the wafer coating; conductive posts formed in the molding resin; and terminals formed on the molding resin. The conductive wiring patterns are electrically connected to the metal pads through the wafer coating. The terminals are connected to the conductive posts one by one.

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According to the conventional chip-size package, a connecting portion (boundary portion) between the conductive post and wiring pattern is extremely narrow and weak. Therefore, the connecting portion may be broken by stress, which is generated when the molding

resin is expanded or contracted.

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According to another conventional chip-size semiconductor package, the connecting portion is shaped to decrease in area gradually from the conductive post to conductive wiring pattern. However, the area to be in contact with the molding resin is increased, so that the molding resin may be easily removed from the conductive post and conductive wiring pattern. As a result, the connecting portion may be broken later.

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OBJECTS OF THE INVENTION

Accordingly, an object of the present invention is to provide a chip-size semiconductor package in which a connecting portion between a conductive post and a wiring pattern is not easily broken.

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Additional objects, advantages and novel features of the present invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

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SUMMARY OF THE INVENTION

According to a first aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; a wafer coat formed over the semiconductor chip; a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern; a molding resin formed over the conductive wiring pattern; a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; and a terminal which is formed on the molding resin and is connected to the conductive post. A connecting portion (boundary portion) of the conductive wiring pattern and conductive post is provided with a slit to disperse stress to be applied to the connecting portion.

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Preferably, the connecting portion is provided with a plurality of slits, which are separated from each other. The slits may be shaped to be rectangular and arranged to extend radially. Preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

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According to a second aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; a wafer coat formed over

the semiconductor chip; a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern; a molding resin formed over the conductive wiring pattern; a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; a terminal which is formed on the molding resin and is connected to the conductive post; and a dummy pattern arranged adjacent a connecting portion (boundary portion) of the conductive post and wiring pattern.

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Preferably, the dummy pattern is a conductive pattern which is formed in the same process as the conductive wiring pattern and is arranged parallel to the conductive wiring pattern. Further, the dummy pattern may include two parts arranged at the both side of the conductive pattern. Further more, preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern, and the two parts of the dummy pattern are arranged along the conductive post and conductive wiring pattern.

【0011】

According to a third aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; a wafer coat formed over the semiconductor chip; a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern; a molding resin formed over the conductive wiring pattern; a

conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; and a terminal which is formed on the molding resin and is connected to the conductive post. At least one of the conductive wiring pattern and conductive post is provided with a dent around a connecting portion (boundary portion) of the conductive wiring pattern and conductive post.

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The dent may be shaped to be square. Preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

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According to a fourth aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; a wafer coat formed over the semiconductor chip; a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern; a molding resin formed over the conductive wiring pattern; a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; and a terminal which is formed on the molding resin and is connected to the conductive post. The conductive wiring pattern is shaped to have a first region extending outwardly from the conductive post and a second region extending vertically from the first region.

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Preferably, the second region comprises a plurality of projecting parts each of which extends vertically from the first region, and the projecting pats of the second region are extended from both sides of the first region. Further, the connecting portion may be shaped to decrease in area gradually from the conductive post to the conductive wiring pattern. At least one of the projecting pats may form a part of the conductive post.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a conventional chip-size semiconductor package.

Fig. 2 is a plan view showing a conventional chip-size semiconductor package.

Fig. 3 is an enlarged view showing a part of the chip-size semiconductor package shown in Fig. 2.

Fig. 4 is an enlarged view showing a part of another conventional chip-size semiconductor package.

Fig. 5 is an enlarged view showing a part of a chip-size semiconductor package according to a first preferred embodiment of the present invention.

Fig. 6 is an enlarged view showing a part of a chip-size semiconductor package according to a second preferred embodiment of the present invention.

Fig. 7 is an enlarged view showing a part of a chip-size semiconductor package according to a third preferred embodiment of the present invention.

Fig. 8 is a cross-sectional view taken on line A-A in Fig. 7.

Fig. 9 is an enlarged view showing a part of a chip-size semiconductor package according to a fifth preferred embodiment of the present invention.

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DETAILED DISCLOSURE OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These preferred embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other preferred embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and scope of the present inventions is defined only by the appended claims.

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~~For better understanding of the present invention, a~~

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conventional technology is first described in conjunction with Figs. 1 to 4. Fig. 1 is a cross-sectional view showing a conventional chip-size semiconductor package 10. Fig. 2 is a plan view showing the conventional chip-size semiconductor package 10, shown in Fig. 1. The chip-size semiconductor package 10 includes a Si chip 12; metal pads 14 formed on the Si chip 12; a wafer coating 16 formed over the Si chip 12; conductive wiring patterns 18 formed on the wafer coating 16; a molding resin 24 formed over the wafer coating 16; conductive posts 20 formed in the molding resin 24; and terminals 22 formed on the molding resin 24. The conductive wiring patterns 12 are electrically connected to the metal pads 14 through the wafer coating 16. The terminals 22 are connected to the conductive posts 20 one by one.

【0018】

Fig. 3 is an enlarged view showing a part 30 encircled by a broken line in Fig. 2. As shown in Fig. 3, a connecting portion (boundary portion) 40 between the conductive post 20 and wiring pattern 18 is extremely narrow and weak. According to the conventional chip-size package, the connecting portion 40 may be broken by stress, which is generated when the molding resin 24 is expanded or contracted.

【0019】

Fig. 4 is an enlarged view showing the part 30 of another conventional chip-size semiconductor package. As described above, a

connecting portion (boundary portion) 140 is a part which is easily broken in response to stress, so that the connecting portion 140 is shaped to decrease in area gradually from a conductive post 120 to a conductive wiring pattern 118.

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However, according to the chip-size semiconductor package, shown in Fig. 4, the area to be in contact with the molding resin 24 is increased, so that the molding resin 24 may be removed from the conductive post 120 and conductive wiring pattern 118. As a result, the connecting portion 140 may be broken easily.

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Hereafter, a preferred embodiment of the present invention is described in detail with reference to Figs. 5 to 9.

【0022】

Fig. 5 is an enlarged view showing the part 30 of a chip-size semiconductor package according to a first preferred embodiment of the present invention. According to the first preferred embodiment, a connecting portion (boundary portion) 240 of a conductive wiring pattern 218 and a conductive post 220 is provided with four slits 250 to disperse stress to be applied to the connecting portion 240. The connecting portion 240 is a part which is easily broken in response to stress, so that the connecting portion 240 is shaped to decrease in area gradually from the conductive post 220 to the conductive wiring pattern 218.

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The slits 250 are arranged to be separated by a predetermined distance from each other. The slits 250 are shaped to be rectangular and arranged to extend radially, as shown in Fig. 5. According to the first preferred embodiment, the slits 250 are provided, so that stress applied to the connecting portion 240 is dispersed, and the molding resin is well in contact or bonded with the conductive post 220 and conductive wiring patter 218. As a result, the connecting portion 240 is not easily broken.

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Fig. 6 is an enlarged view showing the part 30 of a chip-size semiconductor package according to a second preferred embodiment of the present invention. According to the second preferred embodiment, dummy pattern 350 is formed around a connecting portion (boundary portion) 340 of a conductive wiring pattern 318 and a conductive post 320. The dummy patterns 350 are arranged along the shape of the connecting portion 340. The connecting portion 340 is a part which is easily broken in response to stress, so that the connecting portion 340 is shaped to decrease in area gradually from the conductive post 320 to the conductive wiring pattern 318.

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The dummy patterns 350 are of conductive patterns which are formed in the same process as the conductive wiring pattern 318 and are arranged parallel to the conductive wiring pattern 318.

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According to the second preferred embodiment, the dummy patterns 350 are provided, so that stress applied to the connecting portion 340 is dispersed, and the molding resin is well in contact or bonded with the conductive post 320 and conductive wiring patter 318. As a result, the connecting portion 340 is not easily broken.

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Fig. 7 is an enlarged view showing a part of a chip-size semiconductor package according to a third preferred embodiment of the present invention. Fig. 8 is a cross-sectional view taken on line A-A in Fig. 7. According to the third preferred embodiment, a dent 450 is formed around a connecting portion (boundary portion) 440 of a conductive wiring pattern 418 and a conductive post 420. The connecting portion 440 is a part which is easily broken in response to stress, so that the connecting portion 440 is shaped to decrease in area gradually from the conductive post 420 to the conductive wiring pattern 418. The dent 450 is shaped to be square.

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According to the third preferred embodiment, the dent 450 is formed around the connecting portion 440, so that stress applied to the connecting portion 440 is dispersed, and the molding resin is well in contact or bonded with the conductive post 420 and conductive wiring patter 418. As a result, the connecting portion 440 is not easily broken.

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Fig. 9 is an enlarged view showing a part of a chip-size semiconductor package according to a fifth preferred embodiment of the present invention. According to the fourth preferred embodiment, a conductive wiring pattern 518 is shaped to have a first region 518a extending outwardly from a conductive post 520 and second regions 518b each of which is extending or projecting vertically from the first region 518a. The projecting pats of the second region 518b are extended from both sides of the first region 518a. One horizontal line of the projecting pats 518b forms a part of the conductive post 520.

[0030]

The connecting portion 540 is a part which is easily broken in response to stress, so that the connecting portion 540 is shaped to decrease in area gradually from the conductive post 520 to the conductive wiring pattern 518.

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According to the fourth preferred embodiment, the conductive wiring pattern 518 is shaped to have the first region 518a and second regions 518b extending vertically from the first region 518a, so that stress applied to the connecting portion 540 is dispersed, and the molding resin is well in contact or bonded with the conductive post 520 and conductive wiring patter 518. As a result, the connecting portion 540 is not easily broken.